Amendments to the Specification:

In paragraph [0009]:

Spatially predicted coded block patterns have been proposed as an improvement to the conventional intraframe coding standards. In a spatially predicted based intraframe, a macroblock includes four luminance blocks and an associated spatially predicted coded block pattern. The coded block pattern has four bits used for indicating which of the luminance blocks in the macroblock are coded in the bitstream using DCT encoding. To encode a spatially predicted coded block pattern, prediction bits for each bit in the coded block pattern are calculated, each bit in the coded block pattern is XORed with its prediction bit, and the resulting bit pattern ~~formsa~~ forms a spatially predicted coded block pattern. A lookup table is used to convert the convert ~~thespatially~~ the spatially predicted coded block pattern to ~~avariable~~ a variable length code for transmission or storage. The reverse procedure is used to decode the variable length code. A lookup table is used ~~toconvert~~ to convert the variable length code to ~~aspatially~~ a spatially predicted coded block pattern. Prediction bits are calculated for each bit in the spatially predicted coded block pattern and each bit in the spatially predicted coded block pattern is then XORed with its prediction bit.

In paragraph [0017]:

It is therefore a primary objective of the claimed invention to provide a method and apparatus for the parallel calculation of the prediction ~~bitsin~~ bits in a spatially predicted coded block pattern, to solve the above-mentioned problems.

In paragraph [0020]:

It is an advantage of the claimed invention apparatus that after a first clock cycle, the

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bits in the storage ~~devicecan~~ device can be shifted and the first circuit and the second
circuit can ~~bereused~~ be reused for setting the A1 bit and the A3 bit respectively in a
second clock cycle.

5   In paragraph [0060]:

In contrast to the prior art, the present invention calculates the prediction ~~bitsin~~ bits
in a spatially predicted coded block pattern in parallel so that the calculation time is
reduced and the number of clock cycles needed to complete the calculation is reduced. By
splitting the calculation into two clock cycles, the present invention calculates two of the
10   prediction bits for a coded block pattern in parallel allowing a much higher system clock
rate than the prior art and a more efficient solution with minimal components. With the
addition of a NOR-gate, a significant performance gain of 37.5% is achieved by
eliminating the dependency of the A2 bit on the A0 bit during the first clock cycle and the
dependency of the A3 bit on the A1 bit during the second clock cycle. Similarly, if the
15   calculation is executed in a single clock cycle, the present invention calculates the four
prediction bits in parallel allowing a high system clock rate and an efficient solution with
minimal components. The dependency of the A2 bit on the A0 bit and A3 bit on the A1 bit
can be eliminated by adding two NOR-gates to provide a 10% increase in speed for the
A3 bit and a 37.5% increase in speed for the A3 bit.

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In the abstract:

A storage device stores rows of bits including a D0 bit, an X0 bit, an X1 bit, a Y0 bit,
a Y1 bit and a spatially predicted coded block pattern having an A0 bit, an A1 bit, an A2
bit, and an A3 bit. A first circuit is connected to the storage device for setting the A0 bit. A
25   second ~~circuitis~~ circuit is connected to the storage device for setting the A2 bit and
operates in parallel to the first circuit. In a second clock cycle, the bits in the storage
device are shifted and the first circuit and the second circuit are reused to calculate the A1

bit and the A2 bit in parallel. Alternatively, a third circuit and a fourth circuit can be connected to the storage device to calculate the A1 bit and the A2 bit in parallel during the first clock cycle.

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